REMARKS

The present amendment is prepared in accordance with the requirements of 37 C.F.R. § 1.121. A complete listing of all the claims in the application is shown above showing the status of each claim. For current amendments, inserted material is underlined and deleted material has a line therethrough.

For purpose of Appeal, no claims have been amended or added.

No new matter has been added.

Claim Rejections - 35 USC § 103

Claims 1-5, 7-10, 13, 14, 19 and 20

The Examiner has rejected claims 1-5, 7-10, 13, 14, 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. (US Patent No. 6,333,563) in view of Peterson (US Patent No. 5,011,870).

Applicants disagree and traverse this rejection.

Independent claim 1, from which claims 2-4 depend, is directed to a method for assembling an electronic module by attaching a chip to a substrate using a first solder interconnection array and attaching a board to the substrate using a second solder interconnection array such that a space is defined between the board and substrate. The space has a gap height ranging from about 300 microns to about 900 microns, whereby the second solder interconnection array resides entirely within this space. An underfill material is provided within the space prior to applying compressive forces to the electronic module. The underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns

that is present in an amount ranging from about 60 to 64 weight percent. The underfill material directly contacts the board and substrate to maintain the space therebetween and optimize the integrity of the second solder interconnection array during application of compressive forces.

Independent claim 5, from which claims 7-10, 13 and 14 depend, is directed to a method for assembling an electronic module that includes attaching a chip to a substrate using a first solder interconnection array, and attaching an organic board to the substrate using a second solder interconnection array to define a space therebetween. An underfill material is deposited at discrete locations within this space such that the underfill material contacts both the organic board and substrate, as well as selected solder joints, for partially encapsulating the second solder interconnection array at these discrete locations. The underfill is then cured to form a rigid matrix within the space to maintain and enhance integrity of the second solder interconnection array.

Dependent claims 13 and 14 recites that the space has a gap height from about 300 microns to about 900 microns, with the underfill material (in its uncured state) comprising a polymeric material having a filler material present in an amount ranging from about 60% to about 64% by weight per solution, and having a particle size ranging from about 32 microns to about 300 microns in diameter.

Independent claim 19, from which claim 20 depends, is directed to an electronic module assembly that includes a chip attached to a substrate via a first solder interconnection array and a board attached to the substrate via a second solder interconnection array. A space is defined between the board and substrate

with a gap height ranging from about 300 microns to about 900 microns, whereby the second solder interconnection array resides entirely within this space. A rigid matrix of underfill material resides within the space and is in direct contact with the board and substrate for encapsulating the second solder interconnection array to maintain the space and optimize integrity of the second solder interconnection array. This underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns present in an amount ranging from about 60 to about 64 weight percent.

Applicants again submit that Jackson discloses a first set of single melt solder alloy material interconnects 22 joined between the substrate 20 and organic interposer 30, and an underfill 24 of a low melt material filling the exposed area between the substrate 20 and the interposer 30. (Col. 3, ll. 6-41, and Fig. 2.) A second set of interconnect materials 32 having a higher melting temperature are attached to the bottom side of the organic interposer 30 to establish a temperature hierarchy between the higher melting interconnect materials 32 and the low melting underfill material 24. (Col. 3, ll. 25-41.) The interposer is then joined to an organic board 40 using the dual melt material 32. (Col. 3, ll. 42-57 and Fig. 4.) By underfilling the first set of single melt solder alloy material interconnects 22 within this low melting underfill material 24, a key aspect of Jackson is that the interconnects 22 will not melt either when the higher melting interconnect materials 32 are joined to the interposer 30, or when the interposer 30 is joined to the board 40. (Col. 3, ll. 35-41 and col. 4, ll. 7-21.)

The Examiner acknowledges that Jackson does not teach providing an underfill material in the space between the circuit board and the substrate.

To overcome these deficiencies, the Examiner cites Peterson stating that it discloses "an underfill or an encapsulant material used in the process of mounting a solid state electronic device to a circuit board to improve the thermal conductive between the components of the assembly; wherein said underfill material is composed of an organic binder and a filler material having particle size ranging from 20-100 microns and said filler constituting about 40-85 percent of the total weight of the underfill, wherein the a higher thermal conductivity is achieve and thereby avoiding the problems associated with CTE mismatch (Peterson, column 1, lines 13-30, column 2, line 42- column 3, lines 25, column 3, lines 35-40, and column 4, lines 1-34)."

It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have modified the method of Jackson et al. depositing a filler material between the substrate and the board, with a filler material composition as taught by Peterson in order to achieve a higher thermal conductivity is achieve and thereby avoiding the problems associated with CTE mismatch (Peterson, column 1, lines 13-30, column 2, line 42- column 3, lines 25, column 3, lines 35-40, and column 4, lines 1-34).

Applicants disagree and submit that Peterson does not disclose, contemplate or suggest underfill materials for use between a substrate and a board, as is currently claimed. Rather, Peterson is limited to organosiloxanes for use as coatings and encapsulates of electronic devices and the circuit boards on which these devices are often mounted. (Col. 1, ll. 13-18.) That is, the circuit board itself is coated or encapsulated. The compositions of Peterson are "especially suitable as thermally conductive coatings for electronic devices that during their operation generate large amounts of heat which must be dissipated to avoid damaging the device." Col. 5, ll.

38-48.) The Examples of Peterson also show that the compositions disclosed therein are to be applied as smooth, coherent coatings to protect the electronic devices (see, col. 5, l. 54 to col. 7, l. 30) from contact with moisture, corrosive materials and other impurities present in the environment in which these devices operate (col. 1, ll. 18-28), i.e., not as an underfill material between a substrate and a board to maintain the space therebetween and optimize the integrity of the second solder interconnection array therebetween, as is claimed.

Further, Peterson discloses compositions different from that of the present underfill material. As is currently claimed, the present underfill material has a filler material present in an amount ranging from about 60 to 64 weight percent of the underfill material. Peterson discloses a composition of a polyorganosiloxane and a thermally conductive filler, whereby the thermally conductive filler is a mixture that constitutes from 40% to 85% of the total weight of the composition. (Col. 2, l. 58 to col. 3, l. 2.) The upper limit of 85 weight percent of Peterson for the combination of all thermally conductive fillers is based on the mixture of aluminum nitride with a filler having a density of from about 2.0 to 3.0 (col. 3, ll. 3-25), which is different from the density of applicants' underfill material.

In continuing with the differences, Peterson's thermally conductive filler mixture comprises a first filler of aluminum nitride present in the mixture from 20 to 60 weight percent, preferably from 20 to about 50 weight percent (col. 3, ll. 64-66) and having an average particle size no larger than one micron and a second filler having an average particle size of from 10 to 100 microns. (Col. 2, l. 58 to col. 3, l. 2.) Referring to the Examples of Peterson and Table 2, the thermal conductivity of the composition of Peterson is maximized when the weight ratio of the second filler (silicon metal) to the

first filler (aluminum nitride) is 1:1 and 4:1, i.e., the first filler constitutes 20 to 50 percent of the total filler. Referring to Table 2, the composition contains 80 weight percent of the filler mixture, which in the 4:1 ratio comprises 64 weight percent Si metal to 16 weight percent AlN, which does not equate to the composition having a filler with a particle size ranging from about 32 microns to about 300 microns that is present in an amount ranging from about 60 to 64 weight percent of the composition, as is currently claimed. (Col. 7, l. 30 to col. 8, l. 16.) As such, unlike the presently claimed underfill material, Peterson does not teach that its second filler (having particle sizes from 10 to 100 microns) constitutes 60 to 64 weight percent of the composition disclosed therein.

Applicants submit that the combination of Jackson and Peterson does not disclose or suggest an underfill material having such particle sizes and weight percents between a substrate and a board. Moreover, these references, either alone or in combination, do not disclose or suggest also having a mechanical support structure within the space between the substrate and the board (in addition to the underfill material), whereby this mechanical support structure is a bracket (claims 3, 8 and 20), a frame (claims 4, 8 and 20), or even a collar (claim 8 and 20). Jackson in view of Peterson also does not disclose or contemplate only partially underfilling this space to partially encapsulate the second solder interconnection array at discrete locations only (claim 5).

It is for these reasons that applicants submit that claims 1-5, 7-10, 13, 14, 19 and 20 are not obvious over Jackson et al. in view of Peterson.

Claim 6

The Examiner has also rejected claim 6 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 5 above, and further in view of Cui (US Patent No. 6,274,650).

For the reasons as discussed above, applicants submit that claim 5 is not obvious over Jackson et al. in view of Peterson since neither Jackson et al. nor Peterson, alone or in combination, disclose, contemplate or suggest the limitations as recited in claim 5. Cui (US Patent No. 6,274,650) also does not dislcose or suggest an underfill material having the claimed particle sizes and weight percents between a substrate and a board, and as such, does not overcome the deficiencies of either Jackson et al. or Peterson.

Claim 6 is not obvious over the combination of Jackson et al., Peterson and Cui.

Claims 14-18

The Examiner has rejected claims 14-18 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 5 above, and further in view of Kumamoto et al. (US Patent No. 6,632,704).

Again, for the reasons as discussed above, applicants submit that claim 5 is not obvious over Jackson et al. in view of Peterson since neither Jackson et al. nor Peterson, alone or in combination, disclose, contemplate or suggest the limitations as recited in claim 5, and Kumamoto et al. does not overcome these deficiencies.

The Examiner recognizes that neither Jackson et al. or Peterson expressly teach the properties of the underfill material including density, particles size viscosity dynamic tensile modulus as set forth in claims 14-18. To overcome this deficiency the Examiner cites Kumamoto et al. stating that it discloses the properties of a desirable epoxy underfill material applied in a surface-mount processing of an electronic device

for the purpose of relieving significant portions of thermal loads induced by CTE differences between a chip and a substrate (column 1, line 55 – column 2, line 1).

Applicants disagree.

Kumamoto discloses epoxies for filling a gap between a chip and a substrate, which is not what the invention is directed towards. As recognized by the Examiner, Kumamoto discloses an underfill material having a filler material present in an amount ranging from about 80% by weight per solution, with the filler material having a particle size ranging from about 4 to 12 microns. Applicants' specification recites that these conventional underfill materials having filler particle sizes ranging from about 1 micron to about 25 microns in diameter are commonly used to underfill the smaller gap dimensions, and are inadequate as underfill materials for the present larger interconnection grid arrays since they precipitously flow-out from these larger interconnection grid arrays, and thereby leave gaps or voids within such interconnection grid arrays such that the interconnection grid arrays are not entirely encapsulated. (Specification, paragraph [0063].)

The present invention discloses an underfill material having material present in an amount ranging from about 60% by weight per solution to about 64% by weight per solution, and having a particle size ranging from about 32 microns to about 300 microns in diameter. It is submitted that this is a difference in kind, not degree, such that Kumamoto does not rectify the deficiencies of Jackson or Peterson, alone or in combination.

Claims 21 and 22

The Examiner has further rejected claims 21 and 22 under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 1 and 19, and further in view of Morganelli et al. (US Patent No. 7,047,633).

The Examiner recognizes that Jackson et al. and Peterson do not expressly disclose providing a partial underfill material in the interconnection, and cites Morganelli et al. to overcome this deficiency.

Applicants disagree with the rejection of claims 21 and 22, and continue to submit that claims 1 and 19, from which claims 21 and 22 depend, are not obvious over the combination of Jackson et al. in view of Peterson for the reasons discussed in detail above. It is submitted that Morganelli et al. does not overcome these deficiencies since it does not dislcose or suggest an underfill material having the claimed particle sizes and weight percents between a substrate and a board. It is submitted that claims 21 and 22 are not obvious over Jackson et al., Peterson or Morganelli et al., alone or in combination.

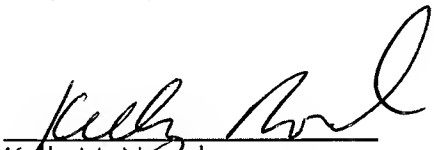
Applicants continue to submit that the suggestion to make the claimed structure, carry out the claimed process and the reasonable expectation of success there-from must be founded in the prior art, not in Applicant's disclosure. *In re Vaech* (CAFC 1991) 20 USPQ2d 1438. The cited reference, and not in retrospect, must suggest doing what Applicants have done. *In re Skoll* (CCPA 1975) 187 USPQ 481. Applicants submit that the cited references, alone or in combination, do not suggest doing what applicants have done, such that applicants' invention would only be found based on applicants' own disclosure, which of course is improper as a hindsight reconstruction of applicants' invention. *Id., W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983) (Hindsight based

on reading of the patent in issue may not be used to aid in determining obviousness). Likewise, hindsight and the level of ordinary skill in the art may not be used to supply a component missing from the cited references. *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 1324, 50 USPQ2d 1161, 1171 (Fed. Cir. 1999).

In view of the foregoing, and under the applicable patent law in this area, it is respectfully submitted that the claims are properly allowable under 35 USC 103.

It is respectfully submitted that the application has now been brought into a condition where allowance of the case is proper. Reconsideration and issuance of a Notice of Allowance are respectfully solicited. Should the Examiner not find the claims to be allowable, Applicants' attorney respectfully requests that the Examiner call the undersigned to clarify any issue and/or to place the case in condition for allowance.

Respectfully submitted,



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